Quasi-Optical VCOs

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***Abstract*—Quasi-optical grid voltage controlled oscillators are presented. These VCOs are the first demonstration of a quasi-optical system consisting of several periodic arrays loaded with solid-state devices. A quasi-optical VCO consists of an array of oscillators, a variable capacitance array, and a mirror. The mirror provides feedback for locked power combining of a large number of MESFET oscillators that load a two-dimensional metal grid on a dielectric substrate. The frequency can be electrically tuned either with gate bias or with another array loaded with varactor diodes. When the varactor bias voltage is changed, the capacitance of the diodes changes, which in turn modulates the frequency of the output power-combined wave. Two types of arrays are presented, one consisting of short dipoles, and the other of bow-tie elements. As expected, the bow-tie VCO has better performance than the dipole VCO, due to its broadband impedance. A 10% tuning bandwidth with less than 2 dB power change was measured in the case of a bow-tie VCO.**

I. Introduction

HIGH FREQUENCY solid-state devices have low output power levels, and the output of a large number of such devices must be combined to achieve high power [1], [2]. Quasi-optical solid-state power combining has generated a lot of interest. Arrays of active patches fed by Gunn diodes and transistors have combined the output powers of up to 16 elements [3]. Recently, two varactor tuned CPW active notch antennas achieved 70% combining efficiency [4] and a second harmonic patch antenna Gunn diode combiner demonstrated a 10.2% isotropic conversion efficiency [5]. Using a Fabry–Perot resonator with a Gaussian beam was proposed in 1986 [6], and such a cavity has been used to combine the powers of several Gunn diodes [7], [8]. A 5 by 5 array of MESFET oscillators was combined in a planar Fabry–Perot cavity at 10 GHz with an ERP of 20.7 Watts and a directivity of 16.4 dB [9]. The largest number of devices combined so far was in a planar grid oscillator in which the individual output powers were combined in free space. This grid oscillator, which operated at 5 GHz, contained 100 MESFETs [10], and similar oscillators using 36 devices were built at C and Ku bands [11], [12]. Planar mixer and amplifier grids have also been demonstrated [13], [14]. The active planar grid structure is versatile in that different components may be designed separately and then combined into one overall system by stacking the two-dimensional grids. In this work, a voltage controlled oscillator consisting of two active grids is presented for the first time.

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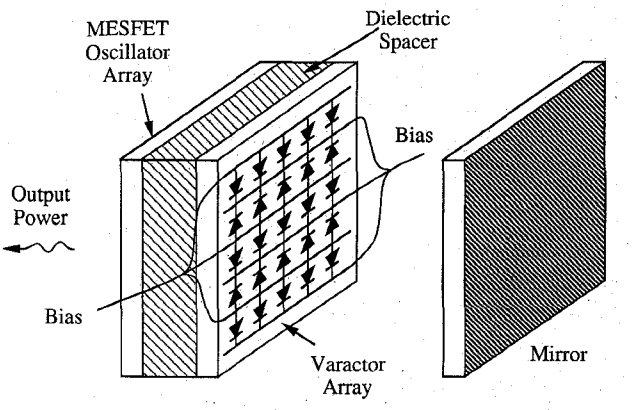

Fig. 1. A quasi-optical voltage controlled oscillator. A grid loaded with oscillating transistors is backed with a grid loaded with varactor diodes. When the capacitance of the diodes is bias tuned, the frequency of the locked oscillation changes. The mirror helps the self-injection locking of the individual oscillators.

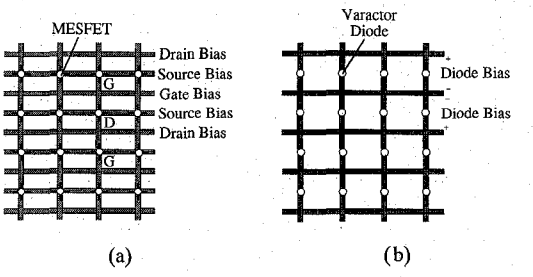

Fig. 2. The dipole (a) MESFET and (b) diode grid structures. The vertical leads radiate, and the horizontal leads are the bias lines.

II. Dipole and Bow-Tie MESFET VCOs

The quasi-optical voltage controlled oscillator shown in Fig. 1 consists of a transistor oscillator grid and a varactor diode tuning grid. The oscillator grid is an array of transistors (Fujitsu FSC11 GaAs MESFETs) arranged on a metallic grid structure, such as the one shown in Fig. 2(a), etched on a 0.5 mm thick Roger's Duroid substrate with $\epsilon_r = 2.2$. Each MESFET is connected to a radiating element on the grid, and the spacing between the transistors is a fraction of a free-space wavelength. For the oscillators presented in this paper, the period is 15 mm and they consist of 7 by 7 arrays of devices. All of the MESFETs in the grids are biased in parallel.

Previous work has shown that the frequency of such an oscillator may be changed mechanically by adjusting the position of the mirror [10]–[12]. However, mechanical tuning is impractical. It is more advantageous to be able to adjust the frequency electrically, particularly for modulation purposes. Electrical frequency tuning can be done by modulating the dc bias of the MESFETs. Another way to tune the oscillation frequency is shown in Fig. 1. A metallic grid structure similar

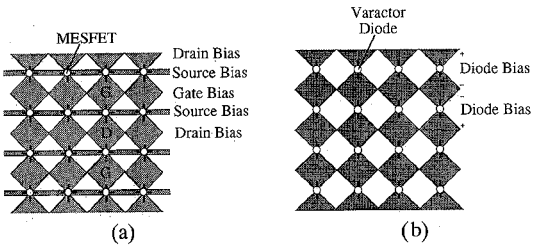

Fig. 3. The bow-tie (a) MESFET and (b) diode grid structures. The horizontal leads on the MESFET grid are source bias lines.

to the transistor grid is loaded with reverse biased varactor diodes. We used Metelics MSV34 varactors that have a specified ratio of $C_{\max}/C_{\min} = 4$. Low frequency measurements of the diode capacitance gave capacitances between 1.7 pF (at 0 V) and 0.7 pF (at 30 V). This diode grid is placed between the oscillator grid and the mirror. The diode reactance changes as the dc bias is adjusted and hence the transistors see a different equivalent impedance. This does not directly affect the bias point of the MESFETs. Both types of electrical frequency tuning will be discussed in this paper.

The oscillation frequency and output power depend on transistor and diode characteristics, grid structure, dielectric spacers, and mirror position. To a large extent, the metal grid geometry determines the frequency of oscillation. One type of grid structure is an array of short dipoles connected to the gate and drain leads of the transistors, as shown in Fig. 2. The driving point impedance of a dipole has a strong frequency dependence. A broadband radiating structure may prove to increase the tuning range. The bow-tie grid in Fig. 3(b) has broadband properties [15], [16], and was built for comparison with the dipole grid. This structure is self-complementary if the array is infinite. This can be seen by first looking at a single feed point assuming there are no generators connected to the other feed points. For this case, the structure is clearly self-complementary and the bandwidth is infinite [17], [18]. By applying superposition, this conclusion extends to the impedances seen by all generators connected to the array feed points. In the transistor grid, Fig. 3(a), the source bias lines perturb the self-complementarity.

The transistor dipole grid was designed using the theory outlined in [10] for the available MESFETs and dielectric substrate. In an infinite grid with all the devices locked in phase, symmetry allows us to represent the grid as an equivalent waveguide unit cell with magnetic walls on the sides and electric walls on the top and bottom. The propagating mode is TEM, and the evanescent modes present reactances at the device terminals. Those reactances are found by the EMF method [19]. The embedding circuit for a device in the grid consists of lead inductances in the gate and the drain, a complex impedance in the source, a 377 Ω transmission line representing free space, and a short representing the mirror. The entire grid is in this way reduced to a one-port equivalent. The measured small-signal transistor s-parameters were used, and the saturation taken into account by reducing $|s_{21}|$ by 2 dB [20]. The reflection coefficient looking into the oscillator from the 377 Ω load is then examined as a function of frequency. When the amplitude of this reflection coefficient is greater than unity and the phase crosses zero, the oscillation frequency is found. For the dipole grid presented in this work, on a 0.5 mm thick dielectric with $\epsilon_r = 2.2$, an oscillation frequency around 3 GHz was found for a grid period of 15 mm and grid leads 1 mm wide. The exact frequency depends on the mirror position and bias. The varactor grid was designed to have the same metal geometry, so that when the two grids are aligned, the unit cell boundary conditions are preserved. The bow-tie grids were made to have the same period as the dipole grids.

Experiments were carried out for mirror tuning, bias tuning, and varactor diode tuning. The varactor diode grid shown in Fig. 1 was only present during the diode tuning measurements and was absent in the case of mirror tuning and bias tuning. In all of the results presented below, the frequency tuning range was limited by either the transistors unlocking, the oscillation ceasing altogether, or the limited capacitance range of the varactors.

III. Mirror and Bias Tuning

For comparison purposes, mechanical tuning using the mirror was performed for each of the oscillator grids. In both cases, less than $\Delta f = 10$ MHz of frequency tuning was observed while the received power varied by $\Delta P = 30$ dB (at broadside) with mirror position. The model described in the previous section shows that the mirror tuning range is smaller when the dielectric is electrically thin, as in our case. Simulations show a tuning range of less than 100 MHz (3%), which is more than in the experiment, possibly due to diffraction loss that is not taken into account in the model. However, when the dielectric constant of the substrate is increased to $\epsilon_r = 10$ in the model, the frequency of oscillation jumps to 4 GHz, and the tuning bandwidth increases to 12%.

Measured radiation patterns with and without the mirror are shown in Fig. 4(a) and 4(b). The dashed line in Fig. 4(a) is calculated for a progressive phase shift $\phi = 2\pi x/7a$ across the seven elements along the horizontal dimension, where α is the grid period. The progressive phase shift gives a difference radiation pattern. In addition, the position of the mirror determines the shape of the radiation pattern, due to the image sources created by the mirror.

Since the transistors are three terminal devices, the bias point is set by both the gate-to-source and the drain-to-source voltages. The drain bias affects both the output power and frequency, but the change in power is much less than in the case of mirror tuning. Drain bias tuning data for the dipole grid oscillating at 2.95 GHz and the bow-tie grid oscillating at 3.18 GHz are shown in Table I. In both cases the output power increased as V_{DS} increased, as expected. The frequency of the dipole grid decreased with increasing drain bias while the opposite was observed for the bow-tie grid. For both grids, the output power is less dependent on gate bias than on drain bias. Gate bias tuning data for the dipole grid oscillating at 2.10 GHz and the bow-tie grid oscillating at 3.50 GHz are shown in Table II. These oscillation frequencies are different in the cases of maximum drain and gate bias tuning, because the two biases do not tune the grids optimally at the same operating points. As shown in Fig. 5, the oscillation frequency

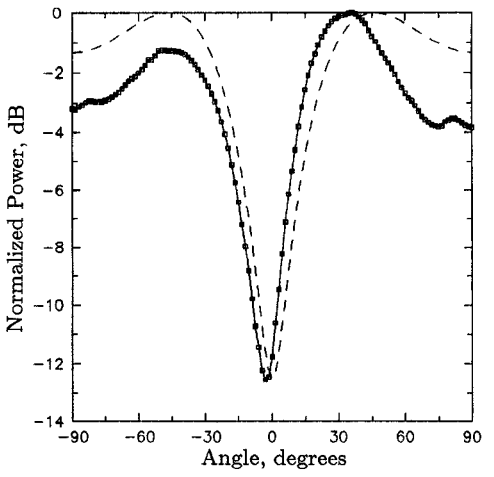

Fig. 4. Oscillator grid radiation patterns for (a) no mirror, E-plane and (b) for grid to mirror spacing of $D = 85$ mm, H-plane. The mirror changes the radiation pattern of the grid. The dashed line in (a) is a calculated pattern corresponding to a progressive phase shift of 2π from one end of the grid to the other.

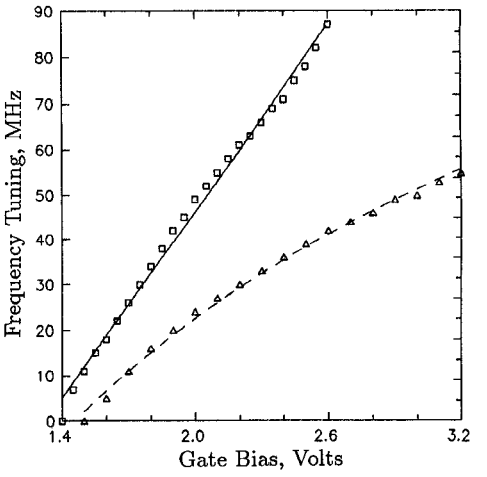

Fig. 5. Gate bias tuning measured for the dipole and bow-tie grids. The grids locked respectively at 2.1 and 3.2 GHz. The solid line shows the dipole, and the dashed line the bow-tie behavior.

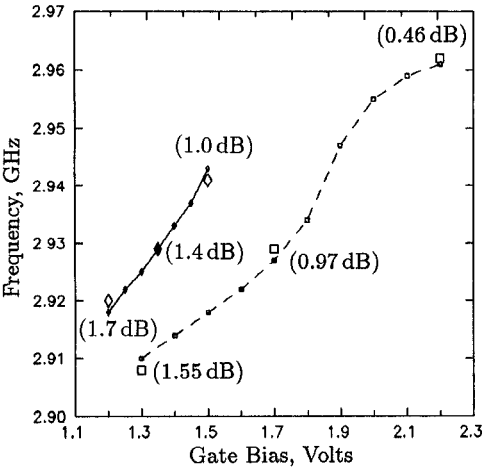

Fig. 6. Measured and simulated gate bias tuning curves of the dipole grid. The solid line shows a 2 V drain bias point, and the dashed line is for $V_{DS} = 3$ V. The respective $|s_{21}|$ parameters for the simulated bias points were decreased by the number given in parentheses next to the corresponding data points.

increases approximately linearly with gate bias. The corresponding change in output power is small. Gate bias tuning was simulated using the circuit model described in [10]. The transistor s-parameters were measured for different bias points, and these were saturated by different amounts for different bias currents. For example, for the dipole grid on a 3.5 mm thick $\epsilon_r = 2.2$ substrate and a mirror spacing of 110 mm, gate bias tuning curves were measured for $V_{DS} = 2$ V and $V_{DS} = 3$ V. Then, the transistor s-parameters were measured with an HP8510 network analyzer for the lowest, highest and a middle current level in each case, using a 50 Ω microstrip test fixture. The $|s_{21}|$ was then decreased by -1.7 dB to $-.5$ dB. Lower saturation was assumed for lower current levels. The obtained tuning points are plotted in Fig. 6, together with the corresponding measured tuning curves. These results show that the gain saturation of the transistors in the grid can be determined from measured gate bias tuning curves and s-parameters of the device.

TABLE I
DRAIN BIAS TUNING DATA FOR THE DIPOLE AND BOW-TIE GRID OSCILLATORS

Grid	ΔV_{DS}	Δ Freq	$\frac{\Delta F}{F}$	Δ Power
Dipole	1.5 V	42 MHz	1.4%	5.5 dB
Bowtie	1.5 V	10 MHz	0.3%	5.7 dB

TABLE II
GATE BIAS TUNING DATA FOR THE DIPOLE AND BOW-TIE GRID OSCILLATORS

Grid	ΔV_{GS}	Δ Freq	$\frac{\Delta F}{F}$	Δ Power
Dipole	1.2 V	87 MHz	4.1%	4.7 dB
Bowtie	1.7 V	55 MHz	1.6%	2.5 dB

IV. VARACTOR TUNING

In the oscillator system of Fig. 1, by varying the reverse bias on the varactors, the capacitance of the diodes, and therefore the frequency of oscillation, are changed. If varactor diodes

TABLE III
VARACTOR DIODE TUNING DATA FOR THE DIODE GRID PLACED BACK-TO-BACK WITH THE OSCILLATOR GRID

Grid	ΔV_{Diode}	Δ Freq	$\frac{\Delta F}{F}$	Δ Power
7 × 7 Dipole	23.0 V	200 MHz	7.1%	24.6 dB
7 × 7 Bowtie	30.0 V	616 MHz	10.3%	12.0 dB
4 × 6 Bowtie	30.0 V	486 MHz	9.9%	2.0 dB

TABLE IV
VARACTOR DIODE FREQUENCY TUNING OF THE OSCILLATORS WITH A 3.5 mm DIELECTRIC SPACER, $\epsilon_r = 2.2$, BETWEEN THE TRANSISTOR AND DIODE GRIDS

Grid	ΔV_{Diode}	Δ Freq	$\frac{\Delta F}{F}$	Δ Power
7 × 7 Dipole	17.0 V	43 MHz	1.7%	5.1 dB
7 × 7 Bowtie	30.0 V	154 MHz	4.2%	14.1 dB

are placed on the same side of the substrate as the FETs, the biasing becomes complicated. If only a few varactors are placed on the back side of the transistor grid substrate, no measurable effect is observed on the frequency tuning. To keep biasing and fabrication simple, in the VCOs presented here, the varactor diodes form a separate grid placed back-to-back with the FET grid. In order to preserve the unit cell waveguide boundary conditions, the varactor grids are made to have the same period as the MESFET grids and the diodes are aligned with the transistors. Since the varactor structure is in the near field of the transistors, the original transmission-line circuit model is no longer applicable. Determining the imbedding impedances and oscillation frequency in this case is a challenging problem.

The behavior of the VCO is sensitive to the electrical thickness of the dielectric between the two loaded grids. The maximum amount of frequency tuning for both the dipole and bow-tie arrays was observed when the transistor and diode grids were placed directly back-to-back, with a 1 mm dielectric of $\epsilon_r = 2.2$ between them. In this case, each transistor is primarily affected by its own diode, and it is difficult to get all of the MESFETs to remain locked. The dipole grid locked at 2.8 GHz, and the bow-tie grid at 6.0 GHz in this case. Tuning data are shown in Table III, and the measured frequency tuning curves for these oscillators are shown in Fig. 7(a). A 9.9% tuning bandwidth around 4.9 GHz with less than 2 dB change in power was measured on an earlier 4 by 6 bow-tie array with a smaller period. In all cases, the polarization of the radiated wave was vertical and not affected by adding the varactor grids. These results indicate the feasibility of a planar broadband voltage controlled oscillator using varactor diodes as tuning elements.

In the previous measurements, the bow-tie and dipole oscillator frequencies and powers were different. Using a dielectric spacer 3.5 mm thick and with $\epsilon_r = 2.2$ between the grids, comparable output power levels were obtained at $V_{DS} = 2$ V. For $V_{GS} = -1.6$ V, the dipole grid locked at 2.6 GHz, and the bow-tie grid locked at 3.7 GHz for $V_{GS} = -2$ V. Table IV lists the resulting tuning data, and the varactor diode frequency tuning curves for the two grids are shown in Fig. 7(b). The bow-tie grid exhibits a wider frequency tuning range.

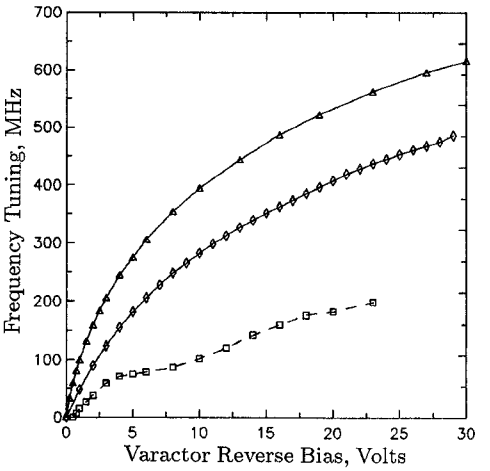

Fig. 7. (a) Varactor diode frequency tuning of three different oscillator grids with the transistor and diode grids back-to-back, and (b) with a dielectric spacer 3.5 mm thick, $\epsilon_r = 2.2$, between the oscillator and diode grids. The squares represent the 7×7 dipole gird, the triangles represent the 7×7 bow-tie grid, and the diamonds represent a 4 × 6 bow-tie grid with a smaller spacing.

This leads to a further issue concerning these tunable oscillators, the tradeoff between bandwidth and output power. Since the drain bias primarily affects the output power, the

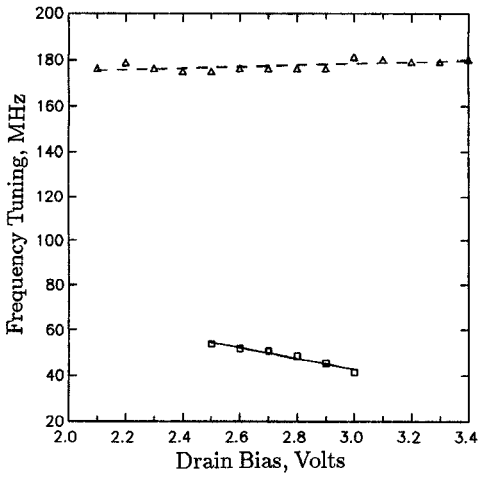

Fig. 8. Measured (a) frequency tuning and (b) relative output power levels for the oscillators as a function of drain bias. The squares represent the dipole grid and the triangles represent the bow-tie grid.

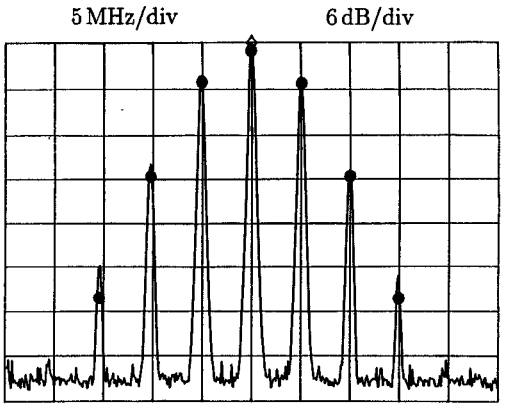

Fig. 9. FM spectrum obtained by modulating the diode bias of the bow-tie grid. The best fit Bessel function coefficients are shown on the plot.

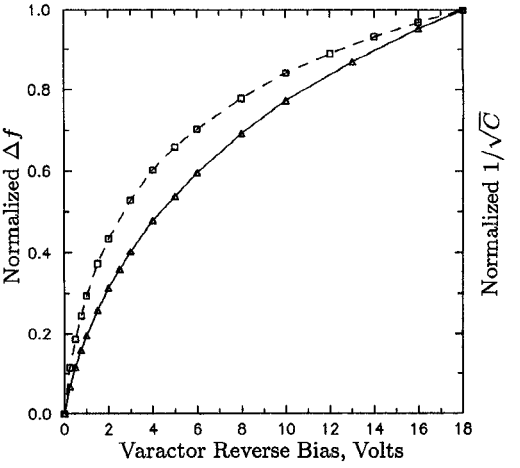

Fig. 10. Normalized $1/\sqrt{C}$ and frequency tuning versus diode bias. The squares represent the normalized $1/\sqrt{C}$, where C is the low-frequency measured capacitance of the diodes, and the triangles represent the normalized measured bow-tie frequency tuning.

amount of frequency tuning and the relative output power levels were measured as a function of drain bias. Fig. 8(a) shows the tuning range at different drain voltages for both grids, and the corresponding power levels are seen in Fig. 8(b). For the dipole grid, it is clear that higher power oscillations result in lower tuning bandwidths. However, this was not seen to be the case for the bow-tie grid, since about 180 MHz of tuning was possible over the entire range of drain bias. The bow-tie grid simultaneously yields more power and a wider frequency tuning range than the dipole grid, and should prove to be a better candidate for a broadband high power voltage controlled oscillator. In addition, the bow-tie grid has better heat-sinking properties.

For frequency modulation of the oscilator, a 5 MHz signal was applied to the diode bias. The resulting FM spectrum is shown in Fig. 9. The corresponding best fit Bessel function coefficient values are also shown in the figure.

For most of the tuning curves, particularly when the two grids are close, the frequency varies in a manner similar to $1/\sqrt{C}$, where C is the measured low-frequency capacitance of the varactor diodes. The frequency of an LC oscillator is determined by $1/\left(2\pi\sqrt{L_{eq}C_{eq}}\right)$, where L_{eq} and C_{eq} are the equivalent inductance and capacitance in the oscillator resonant circuit. Fig. 10 shows normalized frequency tuning curves for the bow-tie grid oscillators (with the transistor and diode grids back-to-back) and the normalzied $1/\sqrt{C(V)}$ dependence on the reverse bias diode voltage, where $C(V)$ is measured at 1 kHz. The difference in the two curves indicates that other reactances also contribute to the VCO frequency vs. varactor voltage dependence.

When the MESFETs and varactors are aligned and the grids are infinite in extent, symmetry defines a unit TEM waveguide cell similar to that in [10]. In this case, an embedding circuit for the transistors in the VCO as shown in Fig. 11(a) qualitatively predicts the behavior of the tuned oscillator. The inductance L represents the gate and drain lead inductance, and the series L_S and C_S represent the source lead reactance. The resistance in all three leads represents coupling to the free-space propagating mode. The variable capacitance C represents the varactor diode. The lead inductances and capacitances are found from the EMF method for the dipole

oscillator grid alone to be $L = 7.0$ nH, $C_s = 0.17$ pF and $L_s = 3.7$ nH. When the varactor grid is added, this type of analysis is not strictly applicable. However, we assumed that the model can be used, provided the capacitance of the varactor couples only to the radiating leads, resulting in the circuit model in Figure 11(a). This equivalent circuit was analyzed using Hewlett Packard's Microwave Design System (MDS), and it was found that for the values given above, and for the measured low frequency capacitance of the diodes between 0.5 and 2 pF (a 1:4 ratio, as specified by the manufacturer), the oscillation frequency was close to the one measured at 3 GHz. When the capacitance C was varied, the normalized frequency tuning curve shown in Fig. 11(b) was simulated. Also plotted in the figure is the measured frequency tuning of the grid versus $1/\sqrt{C(V)}$. This shows that the simple circuit model from Fig. 11(a) qualitatively predicts the behavior of the VCO over the tuning range.

When the diode grid is placed at a distance comparable to a wavelength away from the transistor grid, the varactors have very little effect on either the power or frequency of oscillation. One reason for this can be diffraction loss. The other reason can be seen from the simple transmission line model shown in Fig. 11(c). When the capacitance of the diodes varies over the measured low-frequency range, the phase of the reflection coefficient at 3 GHz varies by only 18°. The reflection coefficient phase change with diode bias was measured between 2 and 3 GHz with an HP8702 Network Analyzer, using a horn antenna connected to the network analyzer port. When the diode reverse bias was varied from 0 to 30 V, it produced about 10° change in phase, as expected from the simple transmission line calculation. In conclusion, diodes of this order of capacitance can affect the oscillation frequency in a useful range only when placed in the near field of the oscillators, as is qualitatively described by the circuit model in Fig. 11(a). For a quantitative model that would allow different metal shapes, such as a bow-tie, the authors feel that a moment method solution is needed, and this is a topic of current research. In the meantime, Hewlett-Packard's High Frequency Structure Simulator (HFSS) was used to obtain electric field intensity distributions for two different bow-tie VCO unit cells, Fig. 12. For both plots, a plane wave is incident on the passive metal-dielectric structure of the grids. Fig. 12(a) shows the electric fields on the bow-tie VCO with a $\epsilon_r = 2.2$ dielectric spacer 3.5 mm thick. Fig. 12(b) shows the bow-tie VCO with an electrically thick spacer, 2.54 cm thick with $\epsilon_r = 9$. The electric field distributions on the transistor and diode grids seem to be less correlated in this case, and a smaller tuning bandwidth would be expected. This was confirmed with measurements using a Stycast slab with the above properties as a spacer. This setup resulted in a 50% narrower tuning bandwidth and an EIRP of around 5 W. This confirms that the dielectric spacer thickness and permittivity are important design parameters from the point of view of electrical characteristics. In a practical application, the spacer also determines the size, as well as the mechanical and thermal stability of the packaged device.

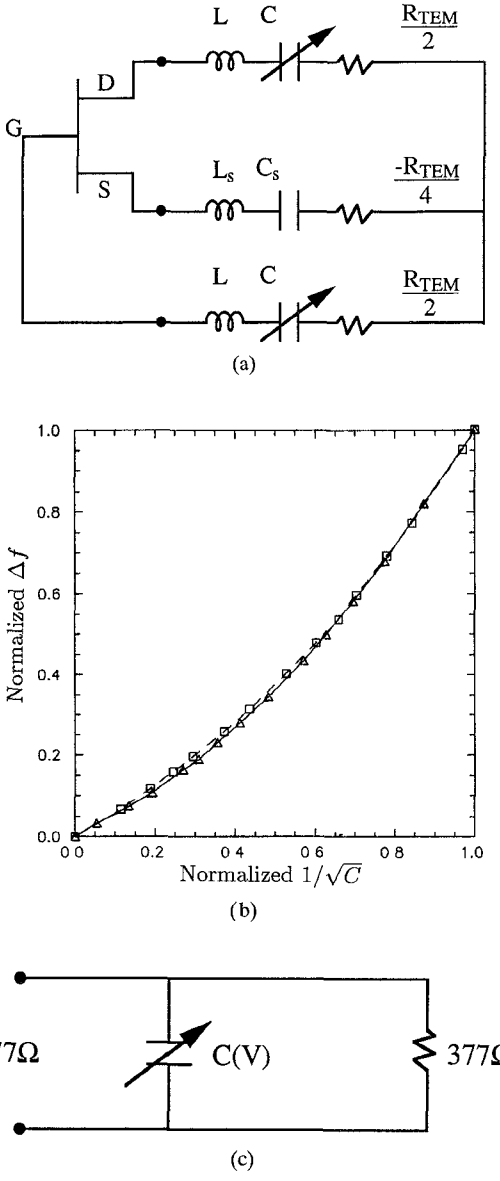

Fig. 11. (a) Equivalent circuit for VCO grid analysis. (b) Simulated (dashed line) and measured (solid line) frequency tuning of the grid versus $1/\sqrt{C}$. (c) Transmission line model for varactor grid placed in the far field of the oscillator grid, where the 377 Ω load represents free-space.

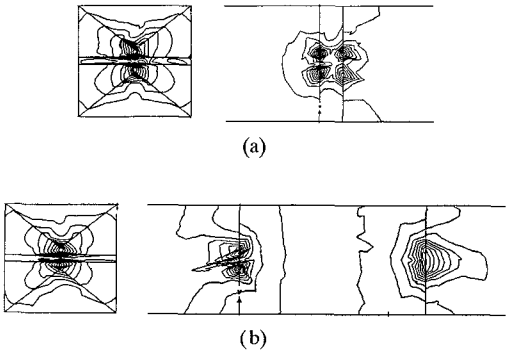

Fig. 12. Transverse and longitudinal electric field intensity contour plots (a) for the bow-tie grid with a 3 mm $\epsilon_{rr} = 2.2$ spacer, and (b) for the bow-tie grid with a 2.54 cm $\epsilon_r = 9.0$ spacer. The asymmetry in the field distribution is due to numerical inaccuracies in HFSS.

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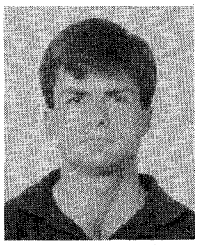

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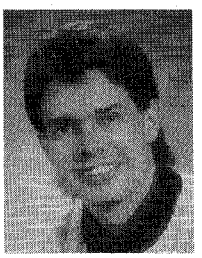

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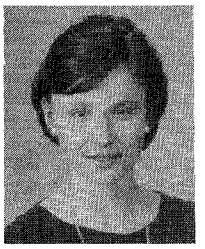

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